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IN THE CLAIMS

Re-write Claims 1, 6 and 20 as follows.

1. (Currently Amended) A semiconductor memory device comprising:

a memory array configured to store data values and corresponding error correction code values;

a first register configured to store a first write data value and a corresponding first write address value during a first write access to the memory array;

an error correction code (ECC) generator configured to receive the first write data value from the first register, and in response, generate a first ECC value during the first write access to the memory array, the ECC generator being configured to provide the first ECC value as long as the first write data value is stored in the first register;

means for outputting the first write data value and the first ECC value during a read access if a read address value associated with the read access matches the first write address value stored in the first register ~~storage circuit~~; and

means for writing the first write data value and the first ECC value to a location in the memory array associated with the first write address value during a second write access.

2. (Previously Canceled)

3. (Previously Amended) The semiconductor memory device of Claim 1, further comprising a second register configured to receive and store the first write data value

and the corresponding first write address value from the first register, and the first ECC value from the error correction code generator, the second register being coupled to the memory array.

4. (Previously Amended) The semiconductor memory device of Claim 1, wherein the means for outputting comprises a comparator coupled to receive the first write address value stored in the first register and the read address value associated with the read access, the comparator asserting a match control signal when the first write address value matches the read address value associated with the read access.

5. (Previously Amended) The semiconductor memory device of Claim 4, wherein the means for outputting further comprises a logic circuit coupled to receive the match control signal and a read enable signal, the logic circuit asserting a hit signal to indicate that a read access has hit the first register when the match control signal and the read enable signal are both asserted.

6. (Currently Amended) The semiconductor memory device of Claim 3 ~~2~~, wherein the first register and the second register form a double buffered write-buffer arranged in a first in, first out (FIFO) configuration.

7. (Previously Amended) The semiconductor memory device of Claim 1, wherein the first register is further configured to store a second write data value and a corresponding second address value during the second write access to the memory array, and wherein the error correction

code (ECC) generator is further configured to receive the second write data value from the first register, and in response, generate a second ECC value during the second write access to the memory array.

8. (Previously Amended) A method of operating a semiconductor memory comprising:

storing a first write data value and a corresponding first write address in a first stage of a write buffer during a first write access;

generating a first error correction code (ECC) value in response to the first write data value stored in the first stage of the write buffer during the first write access and providing the first ECC value as long as the first write data value is stored in the first register;

transferring the first write data value, the first ECC value and the first write address to a memory array during a second write access;

writing the first write data value and the first ECC value to a location in the memory array identified by the first write address during the second write access;

storing a second write data value and a corresponding second write address in the first stage of the write buffer during the second write access; and

generating a second error correction code (ECC) value in response to the second write data value stored in the first stage of the write buffer during the second write access and providing the second ECC value as long as the second write data value is stored in the first register.

9. (Previously Amended) The method of Claim 8, further comprising:

transferring the first write data value, the first ECC value and the first write address into a second stage of the write buffer during the second write access; and

writing the first write data value and the first ECC value from the second stage of the write buffer to the location in the memory array identified by the first write address during the second write access.

10. (Original) The method of Claim 8, further comprising driving the first write data value and the first ECC value to the memory array by enabling tri-state buffers during the second write access.

11. (Previously Amended) The method of Claim 8, further comprising outputting the first write data value and the first ECC value if a read address of a read access matches the first write address value stored in the first stage of the write buffer.

12. (Previously Amended) The method of Claim 11, further comprising inhibiting access to the memory array if a read address of a read access matches the first write address value stored in the first stage of the write buffer.

13. (original) A semiconductor memory device comprising:

a memory array configured to store data/error correction code (ECC) values, wherein each data/ECC

value includes a data value and a corresponding error correction code (ECC) value;

an error detection/correction circuit coupled to receive a first data/ECC value from a first address of the memory array during a first read access, the error detection/correction circuit being configured to generate a corrected first data/ECC value and assert an error indicator signal upon detecting an error in the first data/ECC value; and

a write-back buffer configured to store the corrected first data/ECC value in response to the asserted error indicator signal, the write-back buffer further being configured to write the corrected first data/ECC value to the first address of the memory array during an idle cycle of the memory device.

14. (Original) The semiconductor memory device of Claim 13, wherein the write-back buffer includes multiple entries, and is arranged in a first in, first out (FIFO) configuration.

15. (Original) The semiconductor memory device of Claim 13, wherein the write-back buffer includes multiple entries, and is arranged in a last in, first out (LIFO) configuration.

16. (Original) The semiconductor memory device of Claim 13, wherein the write-back buffer includes multiple entries, the write-back buffer including a circuit to prevent write operations to the write-back buffer when all of the entries of the write-back buffer are full.

17. (Original) A method of operating a semiconductor device, the method comprising:

storing a plurality of data/error correction code (ECC) values in a memory array, wherein each data/ECC value includes a data value and a corresponding error correction code (ECC) value;

generating a first corrected data/ECC value in response to a first data/ECC value retrieved from a first address of the memory array during a first read access, wherein the first data/ECC value includes an error;

asserting an error indicator signal to indicate that the first data/ECC value includes an error;

storing the first corrected data/ECC value and the first address in a write-back buffer in response to the asserted error indicator signal; and

writing the first corrected data/ECC value to the first address of the memory array during an idle cycle of the memory device.

18. (Original) The method of Claim 17, further comprising:

generating a second corrected data/ECC value in response to a second data/ECC value retrieved from a second address of the memory array during a second read access, wherein the second data/ECC value includes an error;

asserting the error indicator signal to indicate that the second data/ECC value includes an error;

storing the second corrected data/ECC value and the second address in the write-back buffer in response to the asserted error indicator signal, wherein the

first corrected data/ECC value and the second corrected data/ECC value are stored in the write-back buffer at the same time; and

writing the second corrected data/ECC value to the second address of the memory array during an idle cycle of the memory device.

19. (Original) A semiconductor memory device comprising:

a memory array configured to store data/error correction code (ECC) values, wherein each data/ECC value includes a data value and a corresponding error correction code (ECC) value;

a write buffer/error correction code (ECC) generator configured to receive and store a write data value and a corresponding write address value, and generate an ECC value in response to the write data value during a first write access;

circuitry for routing the write data value, write address value and ECC value to the memory array during a second write access;

an error detection/correction circuit coupled to receive a first data/ECC value from a first address of the memory array during a first read access, the error detection/correction circuit being configured to generate a corrected first data/ECC value and assert an error indicator signal upon detecting an error in the first data/ECC value; and

a write-back buffer configured to store the corrected first data/ECC value in response to the asserted error indicator signal, the write-back buffer further being configured to write the corrected first

data/ECC value to the first address of the memory array during an idle cycle of the memory device.

20. (Currently Amended) A method of operating a semiconductor memory comprising:

storing a first write data value and a corresponding first write address in a first stage of a write buffer during a first write access;

generating a first error correction code (ECC) value in response to the first write data value stored in the first stage of the write buffer during the first write access;

transferring the first write data value, the first ECC value and the first write address into a second stage of the write buffer during a second write access;

writing the first write data value and the first ECC value from the second stage of the write buffer to a first address in a memory array identified by the first write address during the second write access;

reading the first write data value and the first ECC value from the first address of the memory array;

generating a first corrected data and ECC ~~data/ECC~~ value in response to the first write data value and the first ECC value retrieved from the memory array, wherein the first write data value and the first ECC value includes an error;

asserting an error indicator signal to indicate that the first write data value and the first ECC value includes an error;

storing the first corrected data and ECC ~~data/ECC~~ value and the first address in a write-back buffer in response to the asserted error indicator signal; and

writing the first corrected data and ECC ~~data~~/ECC value to the first address of the memory array during an idle cycle of the memory device.